Claims:

1. A method of implementing a finite state machine in multiple regions with state information communication delays between the regions, the method comprising:

assigning states of the original finite state machine to the multiple regions, the assignment resulting in "border" states which are states that can transition to a state in another region and "adjacent" states which are states that can, within a predetermined number of transitions, transition to a "border" state; and

implementing new finite state machines in each of multiple regions, the new finite state machines including the assigned states and additional states, wherein at least one state of one of the new finite state machines transitions to another state when a communication delayed indication is received that another new finite state machine in a different region was in an "adjacent" state in a prior clock cycle and the finite state machine has a predetermined input history.

2. The method of claim 1 wherein the implementation of the new finite state machines includes duplicate states that allow each element within a region to be controlled by a state within that region.

3. The method of claim 1 wherein the predetermined number is one.

4. The method of claim 3 wherein the communication delay for the state information between regions is approximately one clock cycle.

5. The method of claim 1 wherein the regions comprise slices on a reconfigurable chip.

6. The method of claim 1 wherein the finite state machines for the regions control that region on a reconfigurable chip.

7. A method of implementing a finite state machine in multiple regions, the method comprising:

assigning states of an original finite state machine to the multiple regions; and

implementing new finite state machines in each of the multiple regions, the new finite state machines including the assigned states and at least one wait state, wherein at least one of the new finite state machines includes at least one duplicate state, the duplicate state being entered whenever a matching original state is entered in another of the new finite state machines, the original and duplicate states allowing state information to be provided to more than one region without relying on a communication of state information concerning the matching original state between the more than one region.

8. The method of claim 7, wherein the state information provides control information for elements within the regions.

9. The method of claim 7 wherein there are state information communication delays between the regions.

10. Method of claim 9 wherein the transitions out of the wait-state are done by a delayed indication of the state in another region and a predetermined input history.

11. The method of claim 10, wherein the input history is the previous input to the original state machine.

12. The method of claim 7 wherein the regions comprise slices on a reconfigurable chip.

13. The method of claim 7 wherein the finite state machines implement control for the reconfigurable chip.